Abstract of the Disclosure

Increasing need to gain higher performance and lower power in semiconductor chips and field programable gate arrays requires that optimization be done in a constructive manner with respect to physical layout. Increasing perfomance by parasitic budgeting which dictates what parasitics are acceptable to meet timing and power goals is presented. Providing these controls allows the physical implementation system to skew connection parasitics in a way that makes critical components and their connections significantly faster then those in the rest of the circuit. This represent a unique advantage of existing methods and provide a unique methods to reach higher levels of performance and lower power then existing approaches.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 7, 2004.
(Date of deposit)

Express Mail Receipt Number: EV 104612085 US

Ronald Craig Fish, President
Ronald Craig Fish a Law Corporation
Reg. No. 28,843